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Developing novel low-cost, high-throughput processing techniques for 20%-efficient monocrystalline silicon solar cells

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ABSTRACT

The workhorse of the photovoltaic industry, crystalline-silicon solar cells, continues to have additional headroom for conversion efficiency improvement as well as decreased production costs. As some companies have already demonstrated, clear pathways exist to bring about the achievement of >20%-efficient monocrystalline cells through the use of existing and novel production techniques. A newcomer to the solar cell and module sector, Suniva, has rapidly become a volume manufacturer using innovations originally developed at the University Center of Excellence in Photovoltaics (UCEP) at the Georgia Institute of Technology. This paper discusses the company's first- and second-generation production technologies, including the implementation of ion implantation as a high-volume process, as well as details of cell-making approaches in the development stage.

Introduction

Suniva was founded in August 2007 with the aim of producing high-efficiency crystalline-silicon solar cells based on technology developed at UCEP. After a little more than a year, the company's first commercial solar cell was produced at a newly constructed 30MW per annum manufacturing facility in Norcross, Georgia. The company then expanded capacity to 170MW per annum, with round-the-clock operations producing 156mm pseudosquare cells on p-type Cz wafers with efficiencies of approximately 18%. The company also markets own-branded modules made with its cells; a system equipped with the modules – a 3MW array in India – is shown in Fig. 1. Suniva's cells have also been incorporated into several >1MW ground-mount systems in Italy as well as other locations in the United States and elsewhere.

The company's goal is to produce silicon solar cells and modules with the right balance of cost and efficiency to attain grid parity with fossil fuel-produced electricity at US$0.10/kWh. Levelized cost of energy (LCOE) is a key method for judging the market worthiness of a PV technology since the metric accounts for the total installed system cost and energy production over the life of a PV system. High cell efficiency is arguably the most effective way to shrink LCOE because it reduces the cost of each link in the silicon PV value chain.

Cost modelling summarized in Fig. 2 shows that 18–20% efficient modules at a price of US$1.25/W can produce electricity at US$0.10/kWh. The Solar Advisor Model (SAM) from the Department of Energy's National Renewable Energy Laboratory (NREL) was used for these calculations for a residential PV system in Phoenix, Arizona, using the DOE-projected 2015 balance-of-systems cost of US$2.05/W for a 20% module. Suniva's approach to moving into the US$0.08–0.10/kWh band of grid parity is to raise cell efficiency by building simple yet effective cell structures on commercial-grade monocrystalline silicon wafers without appreciably increasing the number of processing steps and their cost.

Figure 1. Part of a 3MW (DC) grid-connected solar farm, Karnataka, India, the largest utility-owned grid-connected solar project in the country.

First-generation production cells

The first-generation production cells (known as ARTisun) have a traditional

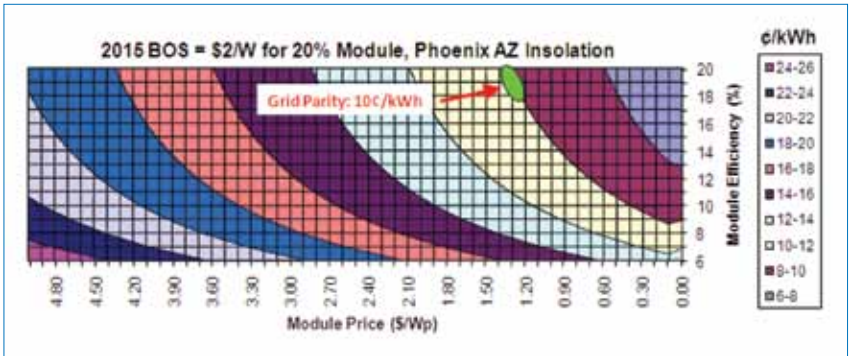
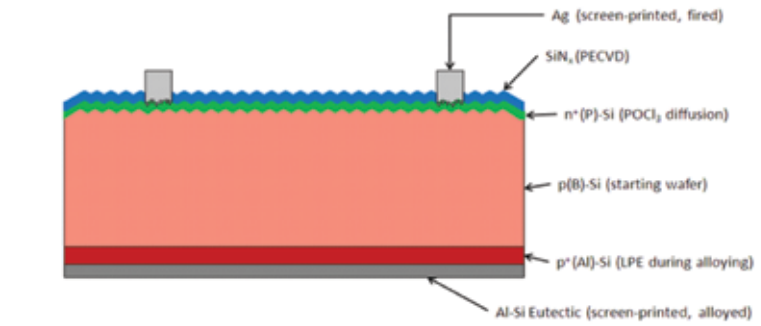


Figure 2. Contour plot of the levelized cost of energy (LCOE) for a residential solar system as a function of module efficiency and price.



Processing Sequence:

1. Saw damage etch/texture
2. $POCl_3$ diffusion (both sides)
3. Removal of phosphosilicate glass
4. SiN_x deposition on front
5. Print/dry back Ag soldering pads
6. Print/dry back Al contact
7. Print/dry front Ag gridlines
8. Co-fire
9. Laser edge isolation

Figure 3. Structure and processing sequence for first-generation production cell ('LPE' refers to liquid phase epitaxy).

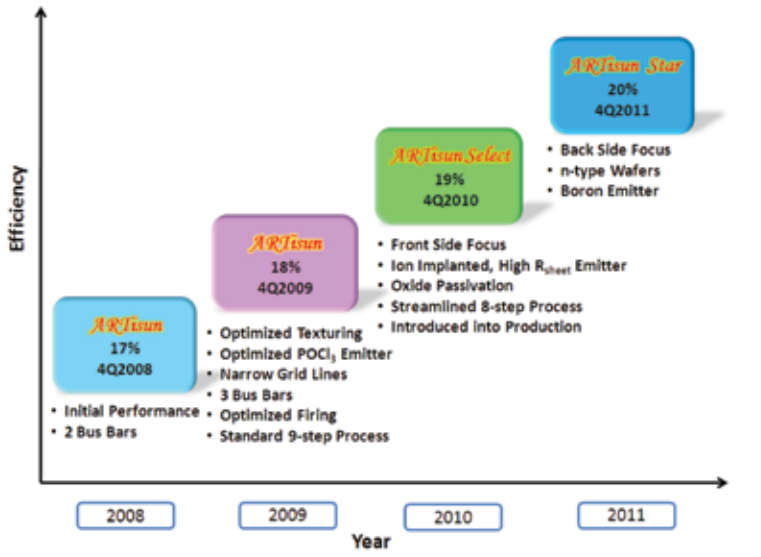


Figure 4. Suniva's roadmap progression from first production in 2008 through three major developments, culminating in 20% production cells in 2011. The first two developments (2009, 2010) have been completed on schedule.

n^+pp^+ structure, with $POCl_3$ emitter diffusion, plasma-enhanced chemical vapour deposition (PECVD) silicon-nitride antireflective (AR) coating, screen-printed and co-fired back-silver, back-aluminium, and front-silver contacts, as illustrated in Fig. 3. Cells are fabricated on 156mm Cz wafers (239cm^2), with an efficiency of approximately 18%. Nine process steps are required, where each step is associated with the wafer travelling through a distinct and major piece of equipment.

Fig. 4 shows the company's technology roadmap for driving the cell efficiency from 17% in 2008 to 20% in 2011. The roadmap calls for three technology developments in three successive years. The first development in 2009 involved optimization of each layer of the basic 17%-efficient screen-printed solar cell. Consistent with the roadmap, optimization was carried out for the surface texturing, for the emitter diffusion and sheet resistance, for the SiN_x AR coating, and for the metal pastes and single-firing cycle used to make screen-printed contacts to the cell. These process improvements reduced reflection and shading to improve short-circuit current density (J_{sc}), provided an excellent aluminium back-surface field (Al-BSF) to enhance the open-circuit voltage (V_{oc}), and produced high-quality contacts with fill-factor (FF) above 0.79. These advances raised the efficiency of the baseline cells from 17% to 18% in 2009, on schedule and at zero additional cost.

Pictures of the front and back of the first-generation production cell are shown in Fig. 5, while Fig. 6 shows the I-V curve. The high FF is characteristic of high-quality contacts and optimum grid/cell design.

Second-generation production cells

Early work at Georgia Institute of Technology resulted in a novel cell process for producing laboratory cells (4cm^2 FZ substrate) with efficiencies up to 20.1%, as measured by Sandia National Laboratories [1,2]. These devices came to be known as 'STAR' cells, an acronym for "simultaneously diffused, textured, in-situ oxide AR-coated." The arrangement for processing these cells is depicted in Fig. 7. A p-type silicon solar cell wafer (S) is located in a quartz boat between a boron source wafer (B) and a phosphorus source wafer (P). On loading the boat into a standard quartz tube, diffusion of boron into one side of the wafer and phosphorus into the other side is accomplished at an elevated temperature in an inert gas. The dopant atoms simply move from the surface of the source wafer to the surface of the solar cell wafer where they are incorporated. After a period of time, the inert gas is changed to oxygen in order to grow a thick thermal oxide for both surface passivation and antireflective coating purposes.

The appeal of this patented process is that it diffuses a phosphorus emitter and a boron back-surface field, and grows a passivating thermal oxide layer all in one thermal cycle using a standard oxidation furnace and with no diffusion glass to strip [3]. It was also found that impurities associated with the dopant coatings on the source wafers largely stayed with the source wafers and were not transported to the solar cell wafer - a sort of 'impurity filtering.' Measured reverse saturation current density (J_{0e}) values for the phosphorus emitter and its surface were quite respectable at 140fA/cm^2 for a 50Ω/sq emitter (limits V_{oc} to 680mV) and 85fA/cm^2 for a 100Ω/sq emitter (limits V_{oc} to 693mV).

Although the STAR process can produce high-efficiency cells, its implementation in volume manufacturing is difficult because the source wafers must be regenerated after each run and the source wafers occupy slots in the boat, which limits the throughput of the solar wafers. However, some of the key advantages of the STAR

Figure 5. Pictures of the front and back of a production cell fabricated from a 156mm pseudosquare Cz wafer.

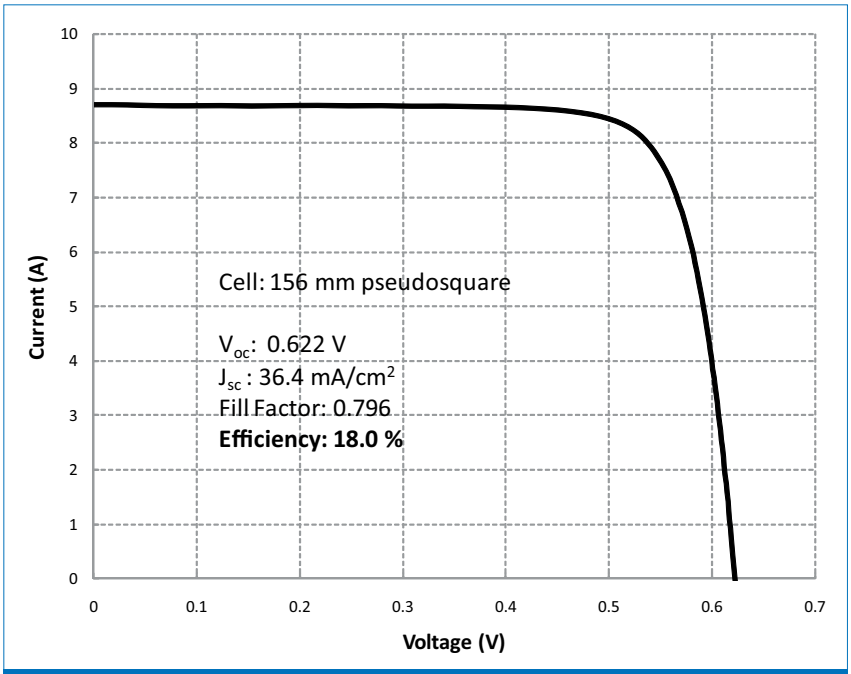


Figure 6. I-V curve for three-bus production cell (239cm²).

process (clean flux of dopant atoms, no diffusion glass formation, in-situ thermal oxide) can be retained in the production-worthy process of ion implantation.

The company has developed a streamlined ion implantation process (known as ARTisun Select) for producing the cell structure shown in Fig. 8. Compared to the $POCl_3$ process, the novel ion implantation scheme reduces the number of process steps from nine to eight. A phosphorus implant step has been added to form a homogeneous emitter, but the phosphosilicate glass removal step and the laser edge-isolation step have been eliminated. Both steps are considered "subtractive", referring to the removal of a material layer created earlier in the process (in this case, phosphosilicate glass (PSG), and an n^+ layer that wraps from front to back of the wafer). Thus, once the saw damage is etched (an unavoidable subtractive step), all other processing steps are additive since the cell structure is built layer by layer. Note that the implant damage must be annealed (step 3), but since this is performed in an oxygen ambient, a passivating thermal oxide is obtained at no additional cost.

Several thousand cells were fabricated in pilot-scale runs prior to introducing this process into full production, with average efficiencies of approximately 19%. The I-V curve of one of the cells produced is provided in Fig. 9. The new process improved the cell efficiency by about 1% (absolute) relative to the $POCl_3$ cell, in conjunction with one fewer processing step. This improvement in efficiency can be attributed to several factors: a highly uniform emitter with elevated sheet resistance; the passivation of that emitter with thermal oxide; excellent screen-printed contacts to the ion-implanted emitter; and the recovery of active cell area by eliminating the laser edge-isolation trench. This required engineering an optimized combination of precise emitter-doping profiles along with metal paste composition and firing to capture the benefits of a lightly doped emitter (37.7mA/cm²), while maintaining a high fill-factor (0.798), as shown in Fig. 9.

The introduction of this novel low-cost, high-throughput manufacturing process is the first instance of ion implantation being introduced into volume production of high-efficiency solar cells. The technique offers several advantages over conventional $POCl_3$ and in-line diffusion technologies including single-side dopant incorporation; in-situ oxidation for superior surface passivation; elimination of the PSG removal step; elimination of the junction edge-isolation step; precise doping control and novel dopant profile engineering by varying implantation dose, implantation energy, and implant damage annealing recipe; and patterned dopant regions for selective emitter and possibly interdigitated back-contact-type cell structures.

Attempts to use ion implantation in solar cell processing are not new: the technique was used in the 1980s to produce small-area R&D-type

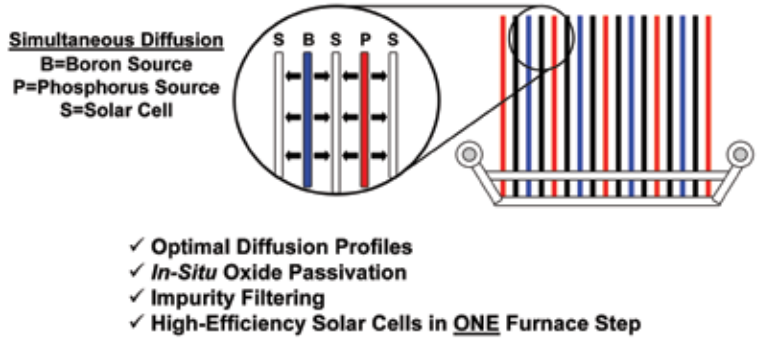


Figure 7. Original STAR process from UCEP, used to produce 20% cell efficiency (4cm² FZ), showing a solar cell wafer sandwiched between a boron source wafer and a phosphorus source wafer in a quartz boat.

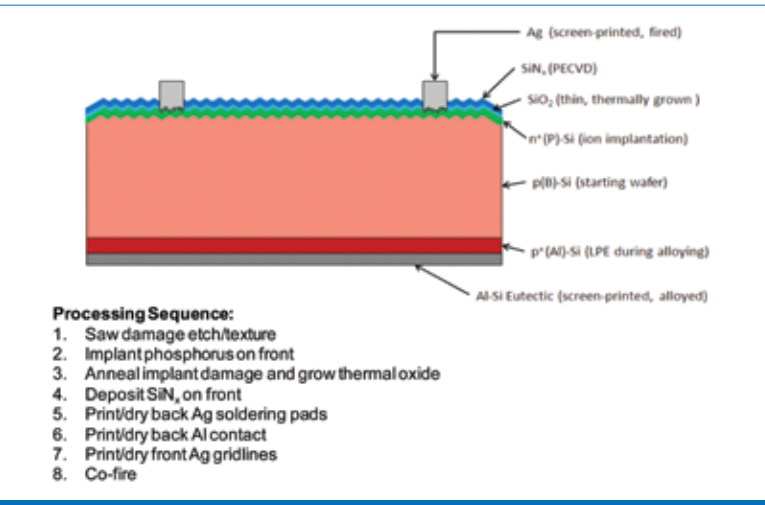


Figure 8. Structure and eight-step fabrication process for ion-implanted cell with homogeneous emitter.

monocrystalline cells [4–7]. However, implantation was abandoned for PV applications because of a common perception that it was too slow and too costly for mass production of silicon cells. Recently, interest in ion-implanted emitters has reawakened [8], with the potential of the implantation technique recognized as a way to produce advanced high-efficiency cell structures with fewer processing steps. In partnership with Varian Semiconductor Equipment Associates (VSEA), which led the development of high beam current, fast wafer handling, high-throughput implanters specifically designed for the PV industry, the potential of this enabling technology was demonstrated through innovation and volume production [9].

A screen-printed selective-emitter cell structure, as shown in Fig. 10, using two in-situ ion implants has also been successfully demonstrated. Firstly, the entire wafer is implanted with a lower dose to create the high sheet resistance field region. A proximity mask is then inserted between the wafer and the ion beam without removing the wafer, and a second implant follows. Openings in the mask define a grid-pattern of heavily doped regions to which the front screen printed contacts must be aligned. As in the case of the homogeneous emitter, the implant damage is annealed in a tube furnace similar to those used for $POCl_3$ diffusions. The process sequence is essentially the same as that for the homogeneous emitter.

In-situ oxidation also helps in contact alignment if this alignment is carried out by pattern recognition. Because the oxide grows much faster on the heavily-doped n-type regions, the grid pattern is easily visible after oxidation. Following the implant anneal, the wafers are sent through a standard PECVD SiN_x deposition step. Since the passivating oxide under the SiN_x contributes to the AR effect, a thinner SiN_x layer is needed which enhances the throughput of the PECVD machine. While most selective-emitter strategies being attempted or used in production require one to four additional steps, the same structure can be achieved with one less process step using the masked ion implantation approach.

The value of an implanted selective emitter over its homogeneous emitter counterpart is clearly seen in the short wavelength range of the internal quantum efficiency data shown in Fig. 11. However, the corresponding efficiency benefit relative to a homogeneous implanted emitter is modest at 0.1–0.2% (absolute) because of the superior ion-implanted homogeneous emitter process, which also produces ~19% cells. An increase in J_{sc} (0.3mA/cm^2) and V_{oc} (2mV) is partially offset by a decrease in FF (0.004) associated with the higher sheet resistance in the field. In the interest of higher implantation

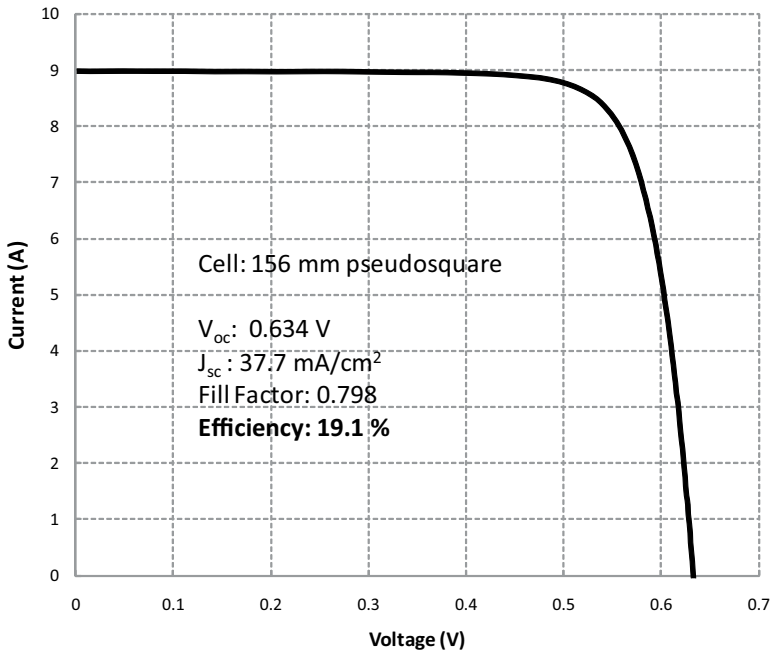


Figure 9. I-V curve of ion implanted cell (239cm^2) with homogeneous emitter.

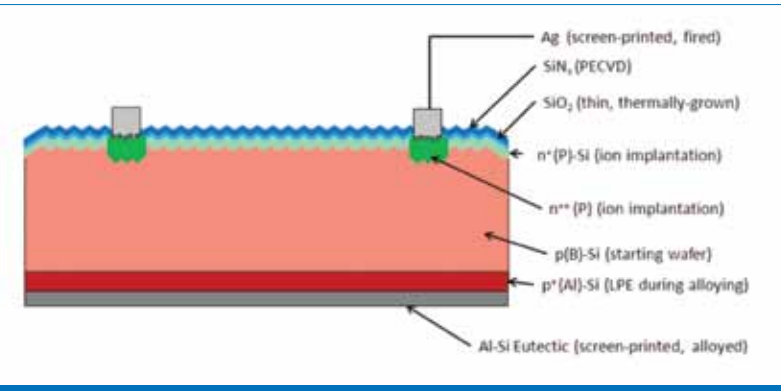


Figure 10. Cell structure with ion-implanted selective emitter instead of a homogeneous emitter.

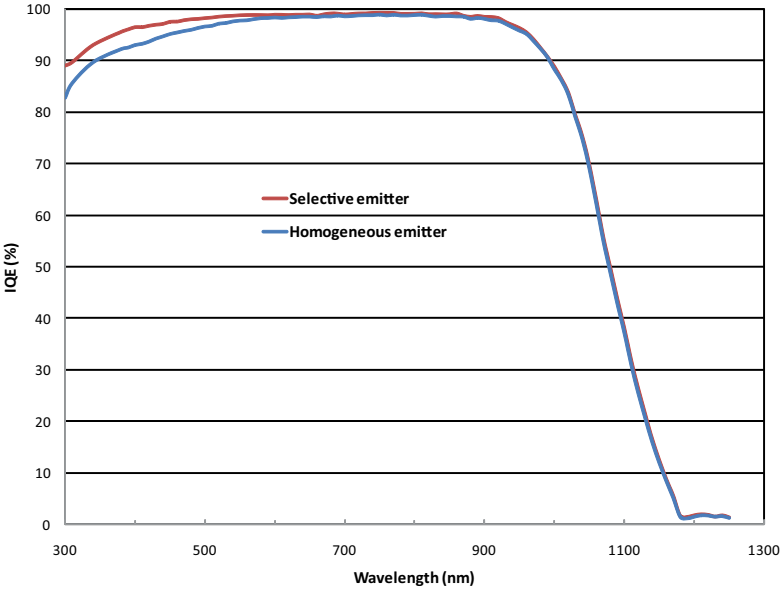


Figure 11. Measured IQE for cells having a homogeneous emitter and a selective emitter.

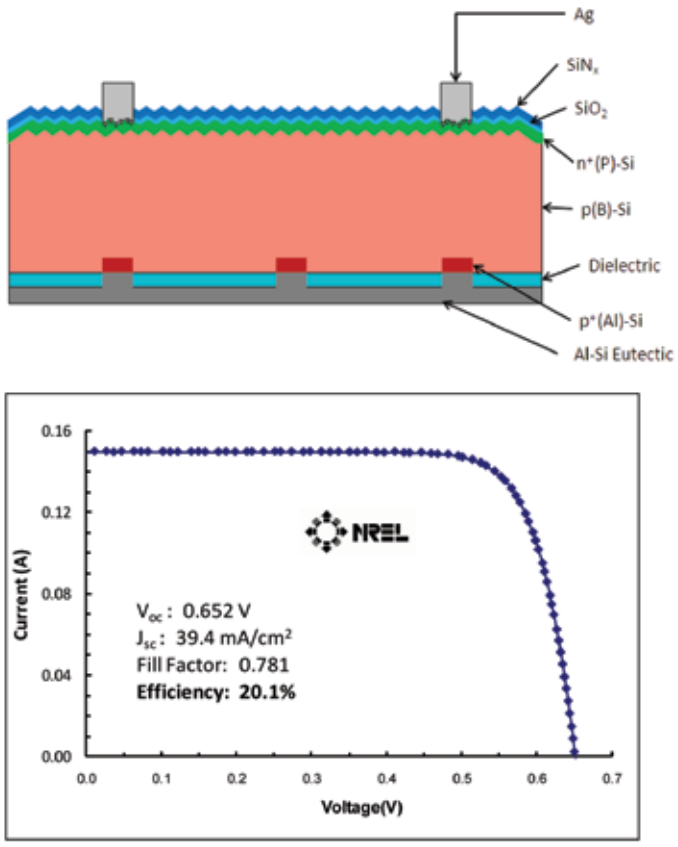


Figure 12. Structure of Delta-STAR cell (top) and corresponding current-voltage performance (4cm² FZ) (bottom).

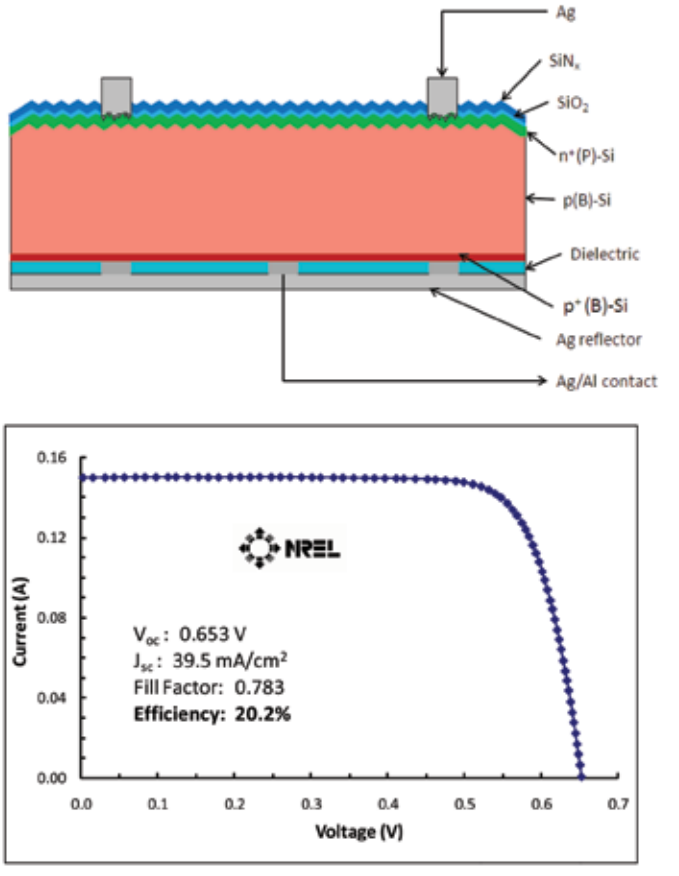


Figure 13. Structure of Beta-STAR cell (top) and corresponding current-voltage performance (4cm² FZ)(bottom).

throughput and simplicity, the production of implanted cells with a homogeneous emitter has begun. In the future, a pattern-recognition approach to grid-line alignment may be adopted to capture the added benefit of the selective emitter.

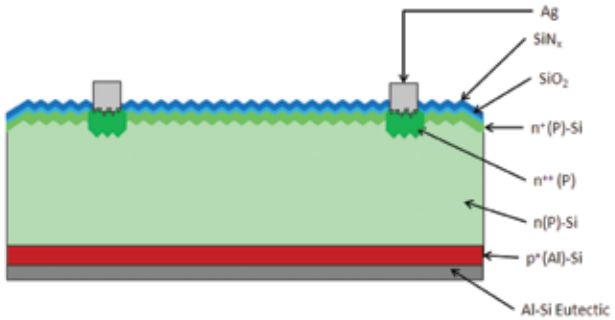
High-efficiency laboratory scale cells

The third development step in the technology roadmap calls for the development of 20%-efficient solar cells with simplified processing and low-cost screen-printed contacts. Detailed characterization and modelling of the 19% full Al-BSF cell shows a back-surface recombination velocity (BSRV, a measure of surface passivation) of 400cm/sec and a back-surface reflectance (BSR, a measure of light trapping) of 65%. In addition, a full Al-BSF results in 0.5% efficiency loss and wafer warpage when the wafers are thinned down to ~120µm. To address these issues, two screen-printed cell structures have been developed (Delta-STAR and Beta-STAR), which include rear dielectric passivation to increase BSR and lower BSRV, while eliminating wafer warpage.

Fig. 12 shows the structure and the corresponding efficiency of the NREL-validated 20% Delta-STAR cell. In this structure, an oxide/SiN_x stack provides the rear passivation and local Al BSF points are formed by opening vias either using a screen-printed etching paste or a laser. An Al paste was screen-printed on the rear side and cofired with the front Ag grid to form the local BSF through the vias without affecting the quality of the oxide/SiN_x stack passivation. The Delta-STAR structure raised the BSR from 65% to 93% and lowered the BSRV from 400cm/sec to 150cm/sec, resulting in 20.1% efficient cells.

Fig. 13 shows a second approach to 20% efficient cells, a feat that involves dielectric passivation of the boron back-surface field (B-BSF), referred to as the Beta-STAR structure. Unlike the Delta-STAR structure where the dielectric has the burden of improving both the BSR and the BSRV, in the second structure a passivated semitransparent B-BSF lowers the BSRV while the metal-capped dielectric provides the enhancement in BSR. Local ohmic contacts are made to the B-BSF by cofiring Ag/Al dots through the rear dielectric and Ag gridlines on the front. In this structure, the dielectric passivation quality does not need to be very high because of the presence of the B-BSF. In fact, detailed analysis showed that the dielectric/BSF interface has a recombination velocity of 45,000cm/sec, which translates into a BSRV of ~140cm/sec at the p/p⁺ interface. This structure also has a BSR of 93% and a cell efficiency of 20.2%, both of which were independently validated by NREL.

Both the Delta- and the Beta-STAR structures have been demonstrated on 4cm²



Processing Sequence:

1. Etch saw damage and texture (100) wafer surface
2. Implant phosphorus for front surface field
3. Anneal implant damage and grow thermal oxide
4. Deposit SiN_x on front
5. Print/dry back Al contact
6. Print/dry front Ag gridlines
7. Co-fire
8. Apply back soldering pads

Figure 14. Cell with phosphorus-doped selective FSF, oxide passivated front surface, and aluminium alloy rear p-n junction.

R&D cells thus far as proof of concept, and work continues to scale up these structures for mass production. In addition, high-efficiency n-type cells are in development as well as a low-cost IBC process.

Initial n-base cells

Fig. 14 shows the structure and processing sequence for a simple n-base cell fabricated from 156mm pseudosquare n-type Cz wafers. This cell is known as 'PhosTop' because the top surface is doped with phosphorus rather than boron, as is usually the case for an n-base cell. The quality, uniformity, and reproducibility of the aluminium alloy p-n junction was shown to be satisfactory for silicon solar cells in 2001, with the first PhosTop cells having an efficiency of 14.2% on Sb-doped dendritic web silicon ribbon [10]. The patent for the structure and fabrication process [11] belongs to Suniva. Since then, other groups have explored this simple structure and process using monocrystalline n-type wafers [12-14].

The PhosTop structure is similar to that of the p-base ARTisun cell shown in Fig. 3. The differences between the two structures is that in the former, the Al-alloyed p-n junction lies at the rear of the cell, the front surface field (FSF) is selectively doped, and the front surface is passivated with a thermal oxide layer. High resistivity n-type wafers are used to ensure sufficiently high lifetime to support a rear-junction cell. Apart from removing the saw damage from the starting wafer, the processing sequence is strictly additive and is accomplished in just eight steps, as illustrated in Fig. 14. The selective phosphorus FSF is formed by a masked implant [9] along with a thermal anneal of implant damage. The front SiO_2 passivation layer is obtained as a by-product of the anneal at no cost. All PhosTop process steps in Fig. 14 are well in hand, except for the last step, which is in development.

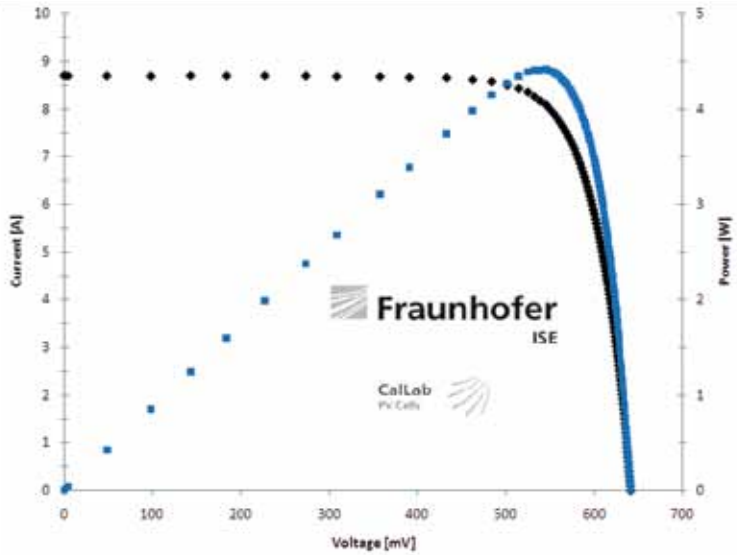


Figure 15. Certified full-area 18.5% cell fabricated from an n-type Cz wafer.

A certified I-V curve from the Fraunhofer Calibration Lab for a 156mm pseudosquare PhosTop cell (239cm^2 area) is shown in Fig. 15. A J_{sc} of 36.4mA/cm^2, V_{oc} of 0.641V, FF of 0.791, and efficiency of 18.5% show the promise of an n-base rear junction cell fabricated by ion implantation. This cell had no solderable back pads. Although small-area (4cm^2) R&D cells with alloyed Al rear emitters have reached 20.0% with amorphous Si passivation of the p^+ emitter surface [15] and 20.1% with Al_2O_3 passivation [16], it is believed that these cells represent the highest efficiency achieved for simple, full-area, production-worthy devices of this type where the alloyed aluminium remains in contact with the p^+ emitter.

Conclusion

Starting initial production with 17% efficient screen-printed p-base cells having $POCl_3$ emitters, Suniva then raised its production efficiency from 17 to 18% on enhanced cells. This improvement was accomplished through optimization of each layer of the traditional cell at zero additional cost. Recently, the company pioneered the use of ion implantation for volume manufacturing of high-efficiency Si cells, starting production of 19%-efficient cells with ion-implanted, high sheet resistance, and homogeneous phosphorus emitters. This technology innovation raised the cell efficiency by another 1% (absolute) while eliminating one complete process step, with improved efficiency attributed to a higher sheet resistance emitter with thermal oxide passivation and the recovery of active front cell area by eliminating laser edge isolation.

A family of ~19% efficient ion implanted selective emitter cells has also been developed, but they offer only a modest improvement in efficiency over the high-performance homogeneous emitter with high sheet resistance. Efforts are under way to scale to volume 20% p-base laboratory scale screen-printed cells, which have been demonstrated at UCEP by improved back surface passivation and reflection. Work on 156mm n-base cells has also begun, with 18.5% top-surface, phosphorus-doped aluminium-alloyed back-junction cells fabricated using a simple process.

Acknowledgments

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Ajeet Rohatgi, founder and CTO of Suniva, is a Regents' Professor and a Georgia Power Distinguished Professor in the School of Electrical Engineering at the Georgia Institute of Technology, where he joined the ECE faculty in 1985 and was founding director of the University's Center of Excellence for Photovoltaic Research and Education. Rohatgi continues his research interests in the development of cost and efficiency roadmaps for attaining grid parity with silicon PV, and innovations in cell design and technology. He received a B.S. in electrical engineering from the Indian Institute of Technology, Kanpur; an M.S. in materials engineering from the Virginia Polytechnic Institute and State University; and a Ph.D. in metallurgy and material science from Lehigh University. Prior to joining the electrical engineering faculty at Georgia Tech, Rohatgi was at the Westinghouse Research and Development Center, and became a Westinghouse Fellow while working on the science and technology of photovoltaic and microelectronic devices. He is an IEEE Fellow and recipient of the William R. Cherry Award, has published more than 370 technical papers in the PV field, and has been awarded 11 patents.

Daniel Meier is chief scientist of Suniva, where he leads the development of new technology and advises on a variety of technical areas. He works closely with the R&D team on new device architectures and processes, and also supports the module side of Suniva's business, providing both technical and application direction. Meier joined the company as one of its first employees in 2007. He holds a B.S. from St. Vincent College and M.S. and Ph.D. from Carnegie-Mellon University, all in physics. He has published more than 75 technical papers in conference proceedings and archival journals, and holds 11 U.S. patents. Meier has also received three Westinghouse Signature Awards for excellence in engineering.

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