High-Efficiency Large-Area Rear Passivated Silicon Solar Cells With Local Al-BSF and Screen-Printed Contacts

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***Abstract*—This paper describes the cell design and technology on large-area (239 cm^2) commercial grade Czochralski Si wafers using industrially feasible oxide/nitride rear passivation and screen-printed local back contacts. A combination of optimized front and back dielectrics, rear surface finish, oxide thickness, fixed oxide charge, and interface quality provided effective surface passivation without parasitic shunting. Increasing the rear oxide thickness from 40 to 90 Å in conjunction with reducing the surface roughness from 1.3 to 0.2 μm increased the $V_{\rm oc}$ from 640 mV to 656 mV. Compared with 18.6% full aluminum back surface field (Al-BSF) reference cell, local back-surface field (LBSF) improved the back surface reflectance (BSR) from 65% to 93% and lowered the back surface recombination velocity (BSRV) from 310 to 130 cm/s. Two-dimensional computer simulations were performed to optimize the size, shape, and spacing of LBSF regions to obtain good fill factor (FF). Model calculations show that 20% efficiency cells can be achieved with further optimization of local Al-BSF cell structure and improved screen-printed contacts.**

***Index Terms*—Passivation, photovoltatics, silicon, solar cells, surface charging.**

I. Introduction

SILICON solar cells with full-area screen-printed aluminum back surface field (Al-BSF) currently dominate the commercial market because of simplicity and lower manufacturing cost. However, this structure has serious limitations of achieving ≥20% efficiencies, especially on thinner wafers. The primary disadvantages of full-area Al-BSF are high back-surface recombination velocity (>300 cm/s) and the low back-surface reflectance (∼65%), which limit the cell performance. In addition, full Al-BSF warps the thin wafers, presenting a barrier to lower cost thinner cells. The high-efficiency passivated emitter with local rear contacts has been made on a laboratory scale to overcome the shortcomings of full-area Al-BSF cells [1]. However, cost-effective production of such cells still remains a challenge [2]. This paper presents the understanding and development of a process sequence that incorporates single-side texturing, optimized front and back oxide/nitride surface passivation, appropriate surface finish, and optimally designed local Al-BSF and contacts to achieve peak efficiency of 19.6% [3]–[7]. This paper highlights the importance and optimization of wet chemical-etching processes for the rear-side planarization, which was studied as a function of surface roughness, light trapping, and surface passivation quality. The second part of this paper addresses the optimization of the oxide thickness and its correlation with surface roughness, which was studied in terms of implied $V_{\rm oc}$, oxide charge $Q_{\rm ox}$, and interface state density or quality (*IQF*). This helped in eliminating the rear parasitic shunting. This is because the desired dielectric layer not only needs to provide high-quality passivation but also contain either a moderate positive charge density or a high negative charge density to avoid the formation of an inversion layer underneath the oxide. The inversion layer gives rise to parasitic shunt if it gets connected to the rear contact points. Besides the necessity of having high quality dielectric, a formation of a high quality and uniform local back-surface field (LBSF) is also important for reducing the parasitic shunt at the edges of back contacts [8]. Finally, a 2-D model was used to perform device simulations to optimize the design and spacing of rear point contacts to minimize the combined effect of resistive and recombination losses.

II. Experiment

Production size 239-cm^2 Si cells were fabricated on 160-μm-thick p-type boron-doped Czochralski (Cz) wafers with a base resistivity of 2.5 Ω·cm. Fig. 1 shows the structure of our Delta-STAR cell which has local Al-BSF through a dielectric rear passivation. This structure gave cell efficiencies of 20% in our laboratory on 4 cm^2, p-type boron-doped float-zone silicon wafer with screen-printed contacts [9], [10]. However, several process modifications had to be performed to achieve high efficiency on commercial grade 239 cm^2 Cz wafers.

The fabrication process begins with saw damage removal in a heated potassium hydroxide solution (chemical formula: KOH) followed by alkaline texturing of both sides of the silicon wafers. To investigate the effect of rear surface roughness on the cell performances, one side of the wafers was planarized using various combinations of alkaline concentration, etching time, and process temperature. Implantation

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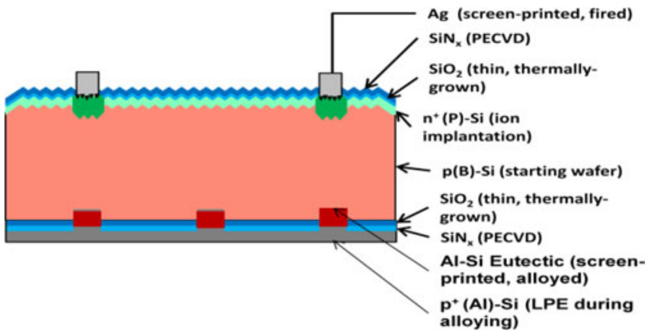

Fig. 1. Structure of Delta-STAR cell with rear dielectric passivation and point contacts.

energy, dose, and anneal conditions were selected to achieve 100 Ω/sq. sheet resistance in the field and 50 Ω/sq. under the grid area of the selective emitter. *In situ* thin oxides were grown on both surfaces during the implant anneal. To investigate the impact of dielectric on the rear passivation, three different oxide thicknesses in the range of 40–110 Å were grown at 840 °C and studied by a combination of C–V measurements and cell parameters. A plasma-enhanced chemical vapor deposition (PECVD) SiNx film was deposited on the front and rear side to cap the oxide. Then, a UV laser (355-nm wavelength with nanosecond pulsewidth) was used to open vias through the rear dielectric stack. Finally, Ag grid was screen printed on the front and fritless Al on the rear dielectric followed by cofiring in a belt furnace. Notice that the cell had no solderable back pads.

The effect of surface roughness of the planarized rear side of the cells was studied using confocal laser microscopy and the long-wavelength reflectance measurements. The dielectric passivation was monitored using the effective minority carrier lifetime measured by Sinton's quasi-steady-state photoconductivity method [11]. The oxide charges Q_{ox} and interface quality factor (*IQF*) were extracted from the contactless *C–V* measurements using a SemiTest SCA-2500 surface charge probe measurements [12].

III. Results and Discussion

A. Effect of Surface Roughness on Surface Passivation Properties

To study the impact of surface roughness on cell efficiency, Delta-STAR solar cells were fabricated using two planarizing etching recipes resulting in average surface roughness 0.746 and 0.205 μm, respectively, in addition to double-side texturing with no planarization treatment and 1.3 μm surface roughness. The roughness of difference surfaces was calculated according to

$$R_a = \frac{1}{n}\sum_{i=1}^{n}|y_i| \tag{1}$$

where R_a is the arithmetic average of the absolute values of height y_i and n is the sampling points over an evaluation area of 258 μm × 258 μm.

The cell *I–V* characteristics are listed in Table I. All other process parameters were kept the same. The highest cell efficiency of over 19.2% was achieved on the smoothest surface with Recipe A treatment while the double-side texturing (Recipe C) gave the lowest efficiency (17.9%). Table I also shows the cell data for a baseline cell with full Al-BSF and no dielectric passivation. Recipe A gave an open-circuit voltage V_{oc} gain of above 18 mV compared to the baseline full Al-BSF cell. About 8-mV increase in V_{oc} resulted from replacing full Al-BSF by dielectric passivation and another 10 mV resulted from planarizing the back. Cells with the smoothest surface showed the best electrical parameters. In contrast, double-side texturing gave cell performance below the baseline full Al-BSF cell with a significant reduction in all the cell performance. Notice that the highest short-circuit current was obtained for Recipe B. This is partly because smaller amount of silicon surface is etched by Recipe B, resulting in slightly thicker (175 μm) cell that absorbs more photons. Best Recipe A resulted in 150-μm-thick cell. Finally, the fill factor increased monotonically with decreasing surface roughness.

TABLE I
Best IV Results of Cz-Si Delta-STAR Cells With Differently Etched Rear Surfaces

Recipe	Roughness [μm]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
A	0.205	656	38.1	76.8	19.2
B	0.746	650	38.4	75.7	18.9
C	1.301	646	37.1	74.8	17.9
Baseline	-	638	37.0	78.8	18.6

The cell area is 239 cm^2.

The aforementioned planarization study highlights the importance of having an optimized rear surface as it relates to *I–V* parameters. In order to assess the enhanced optical performance of the solar cell, PC1D device modeling program was used to quantify the BSR value by matching the calculated and measured escaped reflectance [13]. The analysis gave a BSR value of ∼65% for the conventional full Al-BSF cell and ∼93% for the Recipe A cell. Notice that cell A has 0.3 mA/cm^2 lower current compared to cell B, in spite of superior BSR. This is partly because cell A is 20 μm thinner than cell B; otherwise, cell A would have been even higher than 19.2%.

B. Combined Effect of the Rear Surface Roughness and Oxide Thickness on Surface Passivation

Next, we studied the combined effect of the rear surface roughness and oxide thickness on surface passivation quality using surface morphologies A and B (see Table I) in conjunction with different oxide thicknesses in the range of 40–110 Å. We measured the fixed oxide charge and *IQF* (proportional to the density of interface state) since they are crucial to the performance of dielectric passivated local Al-BSF solar cells [14]. Low positive charge density in a passivating dielectric is desirable for p-base cells because it can avoid inversion-layer-induced parasitic shunting at the silicon/dielectric interface. High positive charge leads to inversion. In addition, low interface state density gives superior passivation due to the lower surface recombination velocity.

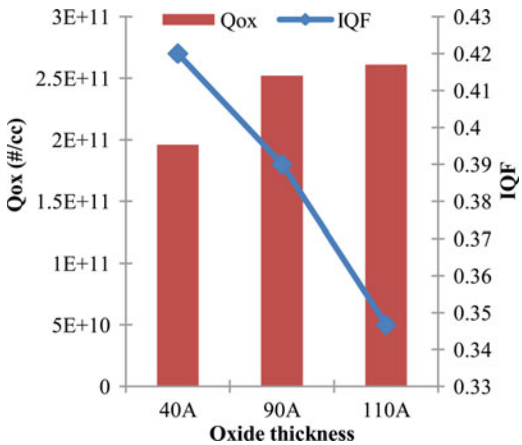

Fig. 2. Effect of oxide thickness on oxide charge and interface quality for an oxide growth on a smooth surface.

The density of the fixed oxide charge $Q_{\rm ox}$ and interface states $D_{\rm it}$ was extracted from the *C–V* measurements on samples using a SemiTest SCA-2500. The SCA measurement is an electrooptical extension of the *C–V* method. It works by shining modulated light on the semiconductor and measuring the resulting ac surface photocurrent. It determines the induced charge per unit area at the semiconductor surface $Q_{\rm ind}$ and the width of the surface depletion layer, W_d. From the set of W_d versus $Q_{\rm ind}$ data collected, the tool computes the oxide charge $Q_{\rm ox}$ and the density of interface states $D_{\rm it}$. When the interface state density is very low ($<10^{10}$ eV^{-1}cm^{-2}), the SCA-2500 provides an *IQF* to characterize the interface states. The *IQF* is given by

$$IQF = \frac{1}{qN_{\rm sc}}\frac{dQ_{\rm ind}}{dW_d} \quad (2)$$

where $N_{\rm sc}$ is the dopant concentration of the wafer being measured, $Q_{\rm ind}$ is the induced charge, and W_d is the depletion width. The *IQF* is related to the interface state density by

$$D_{\rm it} = \left(\frac{\varepsilon_s}{q^2 W_d}\right)(IQF - 1). \quad (3)$$

The *IQF* lies between 0 and 100. A value of 0 represents a perfect interface between silicon and silicon oxide, while a value of 100 represents the worst interface. The detailed derivations of (2) and (3) could be found in [12].

Fig. 2 shows the $Q_{\rm ox}$ and *IQF* for various oxide thicknesses. The thicker oxides showed higher fixed oxide charge density and a slightly lower interface factor, both are good for passivation. High fixed oxide charge exhibits a good field-effect passivation; however, too much positive charge (>2E11/cm^2) may cause inversion and lead to a parasitic shunt if the inversion layer gets shunted by local rear contacts [15].

Fig. 3 shows that the S value for the 90 Å As-grown oxide was 187 cm/s. After the PECVD-SiNx coating, the S value reduced to 122 cm/s. The S value increased only slightly to 135 cm/s after the high-temperature contact firing process (750 °C/s), which should provide appreciable improvement in the open-circuit voltages or efficiency because the full Al-BSF cell has a BSRV value of $\geq$300 cm/s.

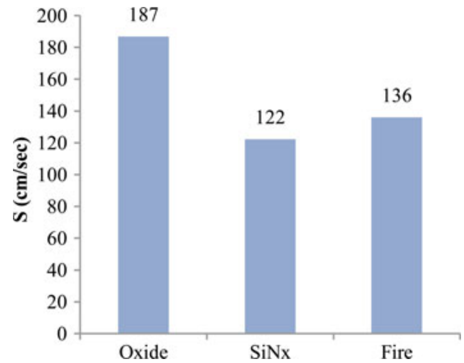

Fig. 3. Surface recombination velocity after the oxide growth, nitride cap and simulated contact firing at ~750 °C.

TABLE II
BEST IV RESULTS OF COMBINED EFFECT OF OXIDE THICKNESS AND SURFACE ROUGHNESS ON CELL PARAMETER OF DELTA-STAR CELLS

Oxide thickness [Å]	Surface roughness [μm]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
40	0.746	640	37.6	74.6	18.0
	0.205	641	37.7	76.0	18.4
90	0.746	652	38.4	77.0	19.3
	0.205	656	38.1	77.8	19.4

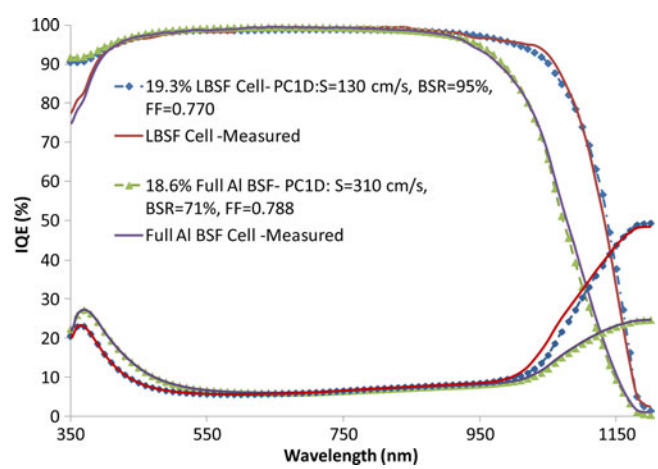

Fig. 4. IQE and reflectance comparison of Delta-STAR and Al-BSF cell. (Solid lines represent measured IQE and reflectance.)

Table II shows that 19.4% efficient Delta-STAR cells (239 cm^2) were achieved on 2.2-Ω·cm Cz Si by a right combination of surface finish and oxide/PECVD-SiNx stack with 90-Å oxide. This LBSF process gave 17-mV improvement with a $V_{\rm oc}$ of 656 mV and 1.1 mA/cm^2 improvement with a $J_{\rm sc}$ of 38.1 mA/cm^2 compared with the baseline full Al-BSF cell. The FF was 77.8%.

In order to explain these improvements, reflectance and internal quantum efficiency (IQE) measurements were performed on a 18.6% efficiency full Al-BSF cell and a 19.3% efficient LBSF cell. It is clear that Delta-STAR cell has much higher BSR and much lower BSRV as indicated by much higher

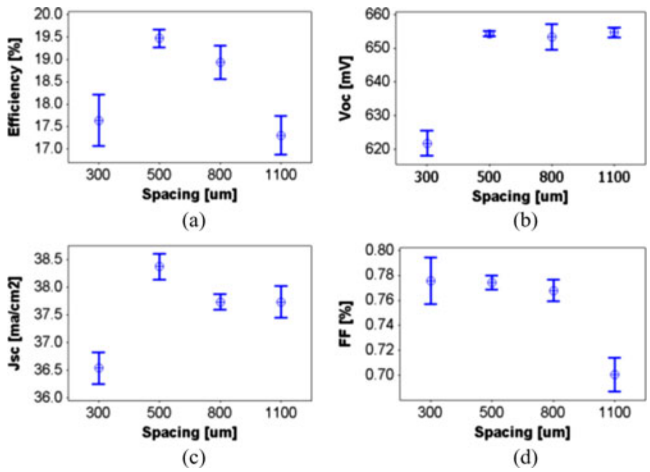

Fig. 5. Experimental data for 239 cm^2 Delta-STAR cells with 130-μm contact width and various contact spacing. Each contact spacing contains five cells.

escape reflectance ($\lambda > 1.0\,\mu$m) and long wavelength IQE ($\lambda > 0.9\,\mu$m) in Fig. 4. PC1D modeling was used to match the experimental *I–V* and IQE data to extract BSRV and BSR values. This analysis revealed an increase in BSR value from 71% to 93% and a decrease in BSRV from 310 to 130 cm/s. Both experimental and model data agreed very well in Fig. 4, using a $Q_{\rm ox}$ value of 2E11 in the dielectric.

C. Effect of Point Contact Spacing on the Rear Side

The aforementioned cells were fabricated with 130 μm $\times$ 130 μm vias with a pitch of 800 μm which was found to be the source of low FF (77.0%) in the 19.3% cell. Therefore, we optimized this contact design using a 2-D device model and established the right combination of the rear contact spacing and opening of the vias [14]. The simulated solar cell efficiency, $J_{\rm sc}$, $V_{\rm oc}$, and FF values were calculated as a function of contact spacing and SRV values at the p-p+ interface for 75- and 150-μm-wide square shaped contacts. Simulations showed that the optimal spacing is smaller for a smaller contact width and the optimal spacing increases with the increase in the effective SRV at the p-p+ interface recombination. This is because optimal spacing is the result of the competition between the resistive and the contact recombination losses [16]. Increasing the spacing increases the resistive loss but decreases the contact recombination, which in turn increases the series resistance and $V_{\rm oc}$ but lowers the fill factor. These calculations gave an optimal spacing of 500 μm for the 150 μm $\times$ 150 μm square openings for a lower SRV value. Fig. 5 shows the corresponding experimental data for $\sim$130 μm $\times$ 130 μm vias which produced the best cell performance of 19.6% at 500 μm spacing for our cells with a BSRV of 130 cm/s and $Q_{\rm ox}$ of 2E11. This is entirely consistent with the 2-D modeling.

Table III shows the cell parameters of 19.3–19.6% efficient Delta-STAR cells with all the optimized parameters, namely 0.205-μm surface roughness, 90-Å oxide thickness, and 500-μm spacing for 130-μm-wide square contacts.

TABLE III
LIST OF 19.3–19.6% OF DELTA-STAR CELLS

ID	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
S-1	656	38.5	77.8	19.6*
S-2	654	38.3	77.7	19.5
S-3	654	38.2	77.0	19.3
S-4	654	38.5	77.2	19.5
S-5	655	38.3	77.6	19.5
S-6	655	38.2	77.2	19.3
S-7	655	38.6	77.4	19.6*
Average	655	38.4	77.4	19.5

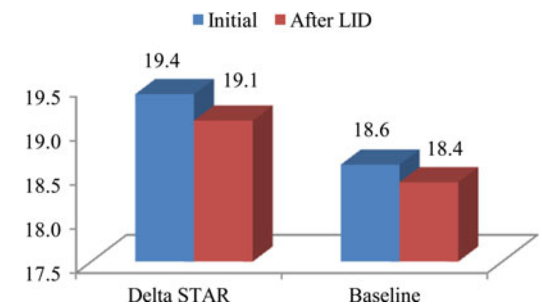

Fig. 6. Post LID efficiency versus initial LID efficiency data for Delta-STAR cells and baseline cells.

Fig. 6 shows the light-induced degradation (LID) in Delta-STAR cell and the baseline Al-BSF cell. The Delta-STAR cell looses $\sim$0.3% (abs.) in efficiency, while the baseline Al-BSF cell drops just $\sim$0.2% (abs.) after 24-h illumination with white light. This confirms our study in [17] that cell designs that improve efficiency by improving surface passivation suffer a greater loss due to LID.

IV. CONCLUSION

This paper shows quantitatively that back-surface finish, rear oxide thickness, dielectric charge and interface quality, and LBSF design, all play an important role in providing excellent back passivation without rear parasitic shunting. This know-how was applied to fabricated cells with all the optimized parameters, namely 0.205-μm surface roughness, 90-Å oxide thickness, and 500-μm spacing for 130-μm-wide square contacts. This resulted in 19.6% efficient, 239-cm^2 screen-printed Cz-Si solar cells with the $V_{\rm oc}$ of 656 mV, $J_{\rm sc}$ of 38.5 mA/cm^2, and FF of 77.8%. This rear dielectric passivation and contact scheme improved the BSR value form 70% to 93% and lowered the BSRV from 310 to 130 cm/s relative to the full Al-BSF reference cell. This is one of the highest efficiency screen-printed 239-cm^2 p-type LBSF Cz-Si solar cells to date.

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Prior to joining the team of scientists and engineers with the University Center of Excellence in Photovoltaics Research and Education, he was with the Integrated Microelectromechanical Systems Group, Georgia Institute of Technology, Atlanta (2006–2008), where he led a team of students and engineers to develop novel fabrication processes for high-frequency micromachined bandpass filters. His interest and deep understanding of semiconductor processing is now being put to work toward the development of low-cost high-efficiency c-silicon solar cells. He is also actively contributing to the development of metallization processes for next-gen cells.

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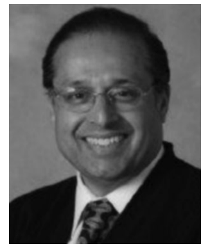
He joined the University Center of Excellence for Photovoltaics, Georgia Institute of Technology, in 2010. His research interests include the fabrication and characterization of screen-printed low-to-medium concentrator silicon solar cells.



Ajeet Rohatgi (F'08) received the B.S. degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 1971, the M.S. degree in materials engineering from the Virginia Polytechnic Institute and State University, Blacksburg, in 1973, and the Ph.D. degree in metallurgy and material science from Lehigh University, Bethlehem, PA, in 1977.

He is currently a Regents' Professor and a Georgia Power Distinguished Professor with the School of Electrical Engineering, Georgia Institute of Technology (Georgia Tech), Atlanta. He is the Founding Director of the University Center of Excellence for Photovoltaic Research and Education, Georgia Tech, and the Founder and CTO of Suniva, Inc., Norcross, GA. Before joining the Electrical Engineering Faculty at Georgia Tech, in 1985, he was a Westinghouse Fellow with the Research and Development Center, Pittsburgh, PA. He has published more than 370 technical papers in this field and has been awarded 11 patents. His current research interests include the development of cost and efficiency roadmaps for attaining grid parity with Silicon photovoltaics (PV), understanding of impurity effects in silicon solar cells, gettering and passivation of defects in solar grade silicon, rapid thermal processing of solar cells, design and fabrication of low-cost high efficiency cells on mono and multicrystalline silicon, and the design, performance and economics of photovoltaic systems.

Dr. Rohatgi is on the Editorial Board of several PV publications and served as the General Chair for the 28th IEEE Photovoltaic Specialists Conference in Alaska in 2000. He received the Westinghouse Engineering Achievement Award in 1985 and the Georgia Tech Distinguished Professor Award in 1996 for his research on high-efficiency solar cells. In 2003, he received the IEEE Photovoltaic Specialists Conference William Cherry Award and the National Renewable Energy Laboratory/Department of Energy Rappaport Award for his contributions to Photovoltaics. In 2007, he received the Georgia Institute of Technology Outstanding Research Program Development Award. In 2008, he was recognized as one of the five most influential people in renewable energy by *Power Finance and Risk Magazine* and by the Georgia Sierra club for his efforts to help move both Georgia and the U.S. into a clean energy economy through his solar energy research at Georgia Tech. In 2009, he received the Invention Award for conservation and pollution-curbing efforts from the Atlanta Business Chronicle, the Climate Protection Award as the Dedication and Technical Innovation in Photovoltaics from the Environmental Protection Agency, and the Hoyt Clark Hottel Award as the Outstanding Educator and Innovator in the field of photovoltaics from the American Solar Energy Society.