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Research

SHORT COMMUNICATION: ACCELERATED PUBLICATION

High-efficiency (19%) Screen-printed Textured Cells on Low-resistivity Float-zone Silicon with High Sheet-resistance Emitters

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High-efficiency 4 cm^2 screen-printed (SP) textured cells were fabricated on 100 Ω/sq emitters using a rapid single-step belt furnace firing process. The high contact quality resulted in a low series resistance of 0·79 Ωcm^2, high shunt resistance of 48 836 Ωcm^2, a low junction leakage current of 18·5 nA/cm^2 ($n_2 = 2$) yielding a high fill factor (FF) of 0·784 on 100 Ω/sq emitter. A low resistivity (0·6 Ωcm) FZ Si was used for the base to enhance the contribution of the high sheet-resistance emitter without appreciably sacrificing the bulk lifetime. This resulted in a 19% efficient (confirmed at NREL) SP 4 cm^2 cell on textured FZ silicon with SP contacts and single-layer antireflection coating. This is apparently higher in performance than any other previously reported cell using standard screen-printing approaches (i.e., single-step firing and grid metallization). Detailed cell characterization and device modeling were performed to extract all the important device parameters of this 19% SP Si cell and provide guidelines for achieving 20% SP Si cells. Copyright © 2005 John Wiley & Sons, Ltd.

KEY WORDS: screen-printing; Si solar cells; high sheet-resistance emitter; surface texture; high-efficiency cells

1. INTRODUCTION

The cost and performance targets of Si photovoltaics can be reached simultaneously by enhancing cell efficiency while utilizing low-cost high throughput processing.[1] Through the use of high-cost cell processing and design, it has been shown[2,3] that the combination of front-surface texturing and high

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sheet-resistance emitters with good surface passivation can significantly enhance the solar cell performance. However, both the advanced design features have not yet been successfully implemented together into the widely used low-cost screen-printing cell technology, which involves a single-step diffusion, plasma-enhanced chemical vapor deposited (PECVD) SiN_x antireflection (AR) coating deposition, and co-firing of the front and back SP contacts. This is because it is difficult to obtain low contact resistance and avoid junction shunting or leakage when dealing with screen-printing technology on shallow junction high sheet-resistance emitters on a textured surface. We have previously demonstrated high fill factors (FF) (>0·78) on high sheet-resistance planar emitters through understanding and optimization of Ag paste and firing recipe.[4] This led to the fabrication of 17·4–17.5% efficient solar cells on float-zone (FZ) Si with SP contacts on an untextured or a planar 100 Ω/sq phosphorus-doped emitter, which represented about 0·5% increase in absolute efficiency over the conventional 45 Ω/sq emitter cells. In this study, we report on the high-efficiency 4 cm^2 SP cells (higher than any other previously reported cell using standard SP approaches) on FZ Si achieved by the combination of surface texturing and high sheet-resistance emitters with good surface passivation.

2. EXPERIMENTAL

In this study, single-crystal SP n^+-p-p^+ solar cells (4 cm^2) were fabricated on p-type, 300-μm thick, (100) textured FZ Si substrates with base resistivities of 0·6 and 1·3 Ωcm. In selected cases planar substrates and 45 Ω/sq emitters were also used for comparison and control. Both textured and planar FZ Si wafers received a standard RCA clean followed by $POCl_3$ diffusion to form the n^+ emitter. A diffusion temperature of 843°C was used for the 100 Ω/sq emitter while 878°C was used for the 45 Ω/sq. The 100 Ω/sq emitter has a surface concentration of $\sim 1{\cdot}48 \times 10^{20}$ cm^3 and a junction depth of $\sim 0{\cdot}28$ μm measured by spreading resistance. The emitter was formed by one step $POCl_3$ diffusion. After the phosphorus-glass removal and another clean, 50 KHz plasma-enhanced chemical vapor desposited (PECVD) SiN_x AR coating was deposited on the emitter. Next, an Al paste was SP on the backside and dried at 200°C. The Ag grid was then SP on top of the SiN_x film, and then the Ag and Al contacts were co-fired (single firing step) in a lamp-heated three-zone infrared belt furnace. Nine 4 cm^2 cells were fabricated on a 4-inch diameter wafer and then isolated using a dicing saw prior to a final 400°C 15 min forming-gas anneal. The cell performance was analyzed by light and dark I-V, Suns-V_{oc} and internal quantum efficiency (IQE) measurements coupled with device modeling.

3. RESULTS AND DISCUSSION

In this study, solar cells were fabricated on planar Si with 45 Ω/sq emitter as well as textured Si with 100 Ω/sq emitter to assess the combined effect of texturing and high sheet-resistance emitter. Table I shows the data for 0·6 Ωcm FZ Si cells with 45 Ω/sq emitter and no surface texturing. These cells were ~17·0% efficient with V_{oc} of 638 mV and J_{sc} of 33·5 mA/cm^2. Regular pyramid texturing was performed by KOH-isopropanol alcohol texturing.[5] Figure 1 shows that the measured average weighted reflectance of a textured SiN_x-coated surface is ~3·2%, which is much lower than the average-weighted reflectance of ~11–12% for a planar SiN_x-coated surface. Such a reduction in front-surface reflectance can lead to a >2 mA/cm^2 increase in photocurrent and 0·85% increase in cell efficiency. Model calculations were performed using the PC1D modeling program[6] to estimate the benefit of a high sheet-resistance emitter. Model calculations in Figure 2 show that 100 Ω/sq emitter with good surface passivation (front-surface recombination velocity (FSRV) of 60 000 cm/s) can contribute to ~0·7% increase in cell efficiency relative to a 45 Ω/sq emitter cell. If the FSRV value for the 45 Ω/sq emitter is much higher (180 000 cm/s), which is often the case because of higher surface concentration, then the improvement over the 45 Ω/sq emitter could be ~1·2% in absolute cell efficiency. In order to validate the above predictions, we fabricated and analyzed SP cells with 100 Ω/sq emitters and regular pyramid texture. As predicted by the models, 18·5%–19·0% efficient FZ Si cells were achieved on a textured high sheet-resistance (100 Ω/sq) emitter [confirmed at the National Renewable Energy Laboratory (Golden, CO)]. The best cell with 19% efficiency was characterized and modeled using PC1D quasi-one-dimensional device modeling program. One disadvantage of the textured surface is the higher FSRV, resulting from an increase in the surface area

Table I. Cell I-V parameters for planar 45 Ω/sq emitter FZ Si cells

V_{oc} (mV)	J_{sc} (mA/cm^2)	FF	Eff (%)	n factor	R_s (Ωcm^2)	R_{sh} (Ωcm^2)
637	34·07	0·793	17·2	1·07	0·696	38 453
638	33·53	0·793	17·0	1·01	0·794	1 969 822
638	33·68	0·789	17·0	1·03	0·805	658 549
639	33·73	0·786	17·0	1·04	0·810	32 846
638	33·42	0·791	16·9	1·02	0·803	514 927
638	33·50	0·792	16·9	1·03	0·797	103 235

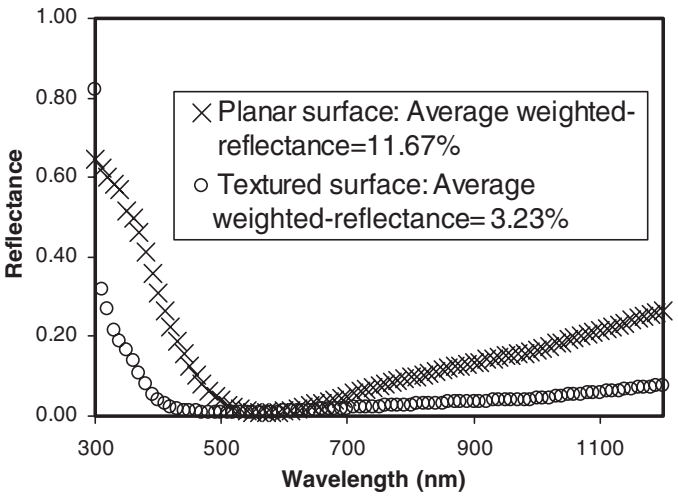

Figure 1. Reflectance of planar and textured emitter surface with SiN_x single-layer AR coating

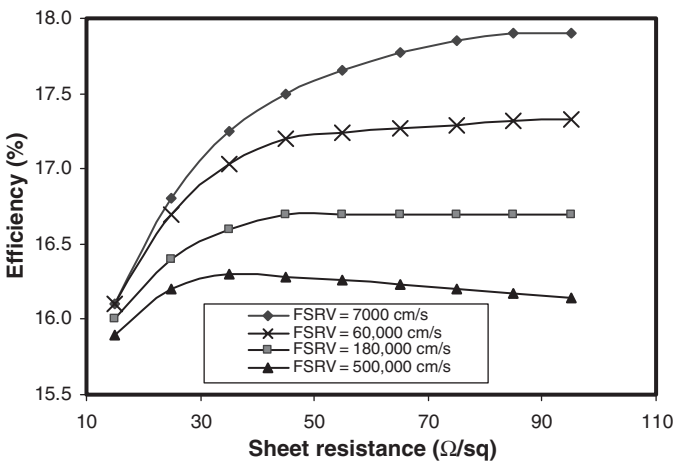

Figure 2. The effect of emitter sheet-resistance and front-surface recombination velocity (FSRV) on planar cell efficiency modeled using PC1D

of the cell. This results in a higher FSRV compared with planar cells.[7] However, raising the sheet-resistance from 45 to 100 Ω/sq may help in lowering the FSRV because it is easier to passivate the surface with lower surface concentration. These efforts are also quantified in this paper through determination of FSRV of textured and planar cells on 45 and 100 Ω/sq emitter cells.

Table II. Light I-V parameters of 0·6 Ωcm textured and planar cells with 45 and 100 Ω/sq emitters

Emitter surface	Emitter (Ω/sq)	V_{oc} (mV)	ΔV_{oc} (mV)	J_{sc} (mA/cm^2)	ΔJ_{sc} (mA/cm^2)	FF	η (%)	$\Delta\eta$ (%)	n factor	R_s (Ωcm^2)	R_{sh} (Ωcm^2)
Textured	45	631	10	36·2	1·3	0·777	17·7	1·1	1·13	0·702	89 026
	100	641		37·5		0·781	18·8		1·09	0·733	68 114
Planar	45	636	10	33·8	0·8	0·789	17·0	0·4	1·03	0·805	658 549
	100	646		34·6		0·780	17·4		1·09	0·789	281 975

Table II shows the light and dark I-V data for the 45 and 100 Ω/sq cells with and without texturing. Table II shows that the 100 Ω/sq emitter textured cell, relative to 45 Ω/sq textured cell gave a V_{oc} enhancement of ∼10 mV, current enhancement (ΔJ_{sc}) of 1·3 mA/cm^2, and absolute efficiency enhancement ($\Delta\eta$) of 0·8%–0·9%. The FFs were similar; indicating comparable contact quality. Short-wavelength IQE analysis in Figure 3 reveals that the enhancement in J_{sc} is largely due to the higher short-wavelength response of the 100 Ω/sq emitter cells, V_{oc} enhancement is due to the combination of higher J_{sc} and lower J_{oe}. Planar cells in Table II also show enhancement due to the high sheet-resistance emitter but the relative efficiency enhancement due to the high sheet-resistance emitter is somewhat lower compared to the textured cells. This is mainly due to the observed greater enhancement in J_{sc} due to the high sheet-resistance emitter in the case of textured cells. In order to understand the reason for this, short-wavelength IQE measurements were analyzed on textured and planar 45 and 100 Ω/sq cells (Fig. 3). By matching the measured short-wavelength IQE with the modeled short-wavelength IQE by PC1D calculations, using the known emitter doping profiles from the spreading resistance measurements, we extracted the effective FSRV values of 90 000 and 150 000 cm/s for the 45 Ω/sq planar and textured cells and 35 000 and 60 000 cm/s for 100 Ω/sq planar and textured cells, respectively. In addition, integrated reflectance, R, of the textured SiN_x-coated surface was found to be ∼3·2% while the planar surface gave an R value of ∼11·7%. Figure 3 shows that the long-wavelength response is the same for all the cells; therefore, the short-wavelengths should account for the difference in J_{sc}. Since $J_{sc}(\lambda) = qN_{ph}(\lambda)(1-R)$IQE and the absolute value of IQE in the short-wavelengths is inversely related to FSRV, the textured cells should have lower IQE compared to their counterpart planar devices. This is supported by the experimental IQE data in Figure 3 and the extracted FSRV values. However, J_{sc} of the textured cells is higher than their planar counterpart, in spite of the higher FSRV, because of the much lower integrated reflectance value (3·2% as opposed to 11·7%). Table II shows that the J_{sc} of textured 45 Ω/sq emitter is 2.4 mA/cm^2 higher than the planar 45 Ω/sq emitter while the J_{sc} of the textured 100 Ω/sq emitter is 2·9 mA/cm^2 higher than the planar counterpart.

To explain the greater enhancement in J_{sc} when a 100 Ω/sq emitter is introduced into a textured cell design compared to the planar counterpart, we need to look at the improvement in the FSRV values for textured and

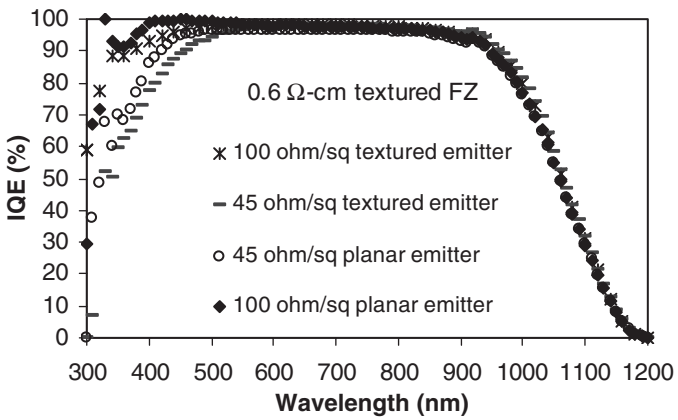

Figure 3. Short-wavelength IQE for 100 and 45 Ω/sq emitter 4 cm^2 cells

planar devices when the 45 Ω/sq emitter is replaced with the 100 Ω/sq emitter. This improvement in FSRV is 90 000 cm/s (150 000–60 000 cm/s) for the textured design while it is only 55 000 cm/s (90 000–35 000 cm/s) for the planar 45 and 100 Ω/sq emitters. This is supported by the cell data in Table II, which shows a 1·3 mA/cm^2 enhancement in J_{sc} for the textured cells while only 0·8 mA/cm^2 improvement in J_{sc} for the planar devices due to the 100 Ω/sq emitter. This is why efficiency enhancement due to the high sheet-resistance is amplified for textured cells (Table II).

Based on the expression of the collection probability of carriers generated close to the surface for homogeneous regions in low level injection,[8] the change in the collection probability with the surface recombination velocity, S, may be expressed as follows:

$$\Delta f_c = -\frac{L\tanh(W/L)}{D\cosh(W/L)\cdot(1+(SL/D)\tanh(W/L))^2}\cdot\Delta S \quad (1)$$

where L is the diffusion length, D is the diffusivity, and W is the distance from the edge of the junction depletion region to the surface. The above equation shows that the greater the change in the surface recombination the greater the change in the collection probability, and therefore the greater the change in the short-circuit current. Moreover, the lower the surface recombination velocity the greater the change in the collection probability. This explains why the 100 Ω/sq emitter cells showed a greater enhancement in J_{sc} than the 45 Ω/sq cells.

Figure 4 shows a distribution of 63 SP textured FZ Si cells fabricated with 100 Ω/sq emitter. Most of the textured cells fabricated on 100 Ω/sq emitters had efficiencies greater than 17·0% with about half the cells with efficiencies in the range of 18%–19%. The few low efficiency cells in Figure 4 resulted from high series resistance (due to a high contact resistance) and poor FF, indicating the need for further optimization of paste and firing conditions. Figure 5 shows the efficiency distribution of nine 4 cm^2 cells (0·6 Ωcm base resistivity) on two 4-inch diameter FZ wafers, measured at NREL using a mask with an aperture area of 3·8 cm^2. One wafer gave all nine good cells with maximum efficiency of 19% while the other had three cells with somewhat lower efficiency. The V_{oc} of the higher efficiency cells was ∼643 mV, which demonstrates that high-quality SP contacts can be achieved on shallow high sheet-resistance textured emitters without shunting. The firing condition was modified slightly for the textured cells based on the optimization for the planar monocrystalline cells. The ramp down rate in the cooling cycle was slowed down slightly, which has been observed to give more uniform results in terms of series resistance due to an improved contact resistance[9] and lower junction leakage current. The specific contact resistance for the textured 100 Ω/sq emitter cell was ∼0·63 mΩcm^2 while that for planar cells with the 100 Ω/sq emitter is typically ∼1–2 mΩcm^2 for the best cases. Commercially available

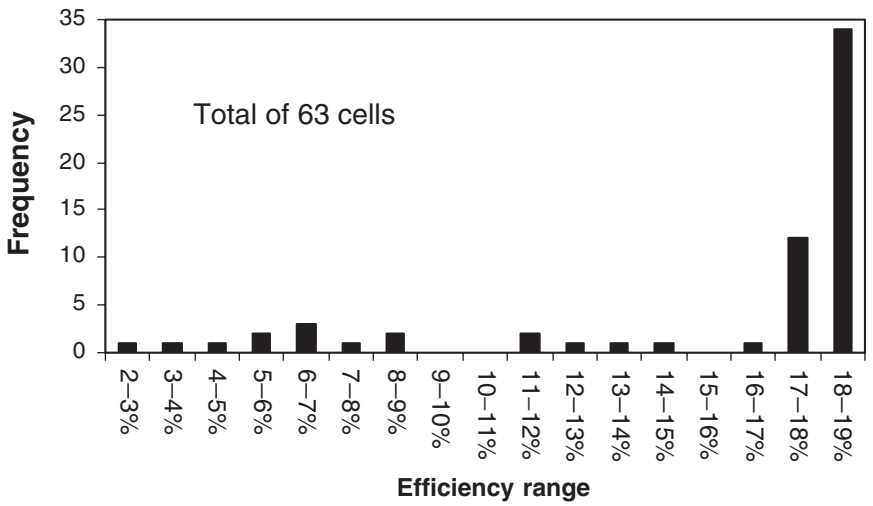

Figure 4. Efficiency distribution of 63 textured (0·6 and 1·3 Ωcm base resistivity) cells with 100 Ω/sq emitters

Figure 5. The distribution of nine 4 cm^2 cells on 4 inch 0·6 Ωcm FZ Si wafers textured on both sides. The V_{oc} ranged form 640–644 mV (measured at NREL)

paste PV168 from DuPont has been used because it has certain properties (glass frit and Ag particle characteristics) which allow it to work very well on high sheet-resistance emitters after a forming gas anneal.[10] These results were supported by the high-quality contact interface, which showed a large number of small Ag crystallites at the interface that are believed to be responsible for the current transport from the Si emitter to the Ag gridline bulk.[11] These Ag crystallites were regularly observed mainly at the edges and peaks of the texture pyramids.[7] The higher surface area per unit volume for the edges and peaks of the texture pyramids, as well as the glass frit-etched surface orientation may have resulted in the larger precipitation of these Ag crystallites at the edges and peaks of the texture pyramids. This behavior generally results in a lower standard deviation in series resistance and a lower macroscopic contact resistivity for the textured compared with the planar high sheet-resistance emitter cells.[7] Another commercially available paste (CN33-455) from Ferro Corp. was also investigated for 100 Ω/sq textured emitters which yielded cell efficiencies of up to ∼18·0% on 1 Ωcm FZ substrates.

In order to understand the performance and behavior of the best cell achieved in this study, a detailed modeling of the 19% cell was performed using several measured key input parameters. The effective FSRV and BSRV values were extracted by matching the measured IQE with the PC1D-simulated data using the measured doping profile (for a planar surface) of the emitter, base doping, and bulk lifetime. The bulk minority carrier lifetime (τ_B) of the 0·6 Ωcm base after the cell fabrication was determined to be ∼250 μs by the photoconductance decay (PCD) technique,[12] after etching the cell down to bare Si. It has been previously shown by device modeling that a lower base resistivity cell gives a higher enhancement in V_{oc} due to the high sheet-resistance emitter compared with a higher base resistivity cell for the same or for a sufficiently high minority-carrier lifetime.[13] The junction leakage current (J_{o2}) of 18·5 nA/cm^2 and second diode ideality factor (n_2) of two were extracted using the Suns-V_{oc} technique.[14] The emitter profile was measured using spreading resistance on a planar 100 Ω/sq emitter and was used in the PC1D modeling of the textured cells. The back reflectance was extracted to be ∼61·5% using an extended spectral analysis of the cell IQE in the long-wavelength range (>950 nm).[15] The grid shading was estimated to be ∼4·5% from the measured ∼75–80 μm wide gridlines on the 2 × 2 cm cell. The FSRV was found to be 60 000 cm/s and back-surface recombination velocity (BSRV) was 600 cm/s from the IQE matching (Figure 6). The FSRV was obtained from the short-wavelength response in the 350–550 nm range. With these input parameters, the PC1D cell modeling (Table III) gave a cell efficiency of 19·0% with $V_{oc} = 640$ mV and $J_{sc} = 37{\cdot}3$ mA/cm^2, which agrees well with the measured data in Table II.

The saturation current density J_{o1} was measured using Suns-V_{oc} for the best solar cells. J_{o1} was found to be equal to ∼433 fA/cm^2 for the best textured cell (19% efficiency) and ∼382 fA/cm^2 for the planar cell (∼17·4% efficiency) fabricated on 100 Ω/sq emitters using PV168 Ag paste. The base saturation current density (J_{ob}) was determined by the following equation:

$$J_{ob} = \frac{qn_i^2}{N_A}\frac{D}{L_{eff}} \tag{2}$$

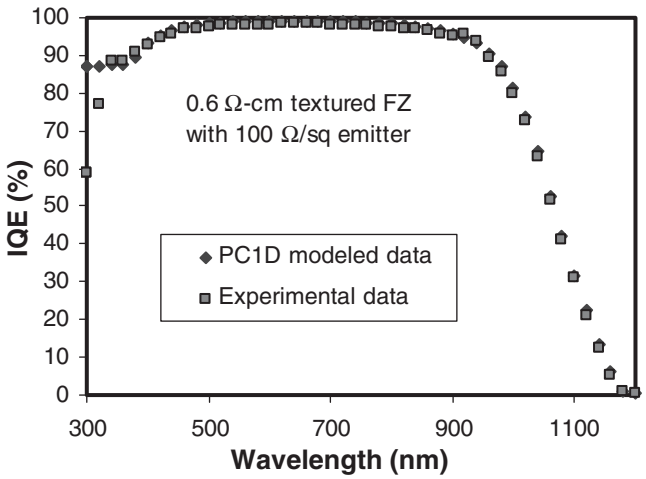

Figure 6. Matching of PC1D-modeled and experimental IQE data

where

$$L_{\text{eff}} = L_{\text{bulk}}/F \tag{3}$$

$$F = \frac{SL_{\text{bulk}}/D + \tanh\frac{W}{L_{\text{bulk}}}}{1 + \frac{SL_{\text{bulk}}}{D}\tanh\frac{W}{L_{\text{bulk}}}} \tag{4}$$

q is the elementary charge, n_i is the intrinsic carrier density, N_A is the acceptor carrier density, D is the diffusivity of minority carriers, and L_{eff} is the effective minority-carrier diffusion length ($L_{\text{eff}} = L/F$), which includes the surface effect (F), and S is the back-surface recombination velocity. J_{ob} was found

Table III. Modeling parameters for the 19% textured 100 Ω/sq cell

Cell parameters	Textured FZ cell
Base resistivity (Ωcm)	0·6
R_s (Ωcm^2)	0·79
R_{sh} (Ωcm^2)	68 157
n_2	1·65
J_{o2} (nA/cm^2)	2
Emitter sheet resistance (Ω/sq)	100
Surface Conc. (cm^3)	$1{\cdot}5 \times 10^{20}$
Texture angle (degrees)	54·7
Texture depth (μm)	3
τ_{bulk} (μs)	250
BSRV (cm/s)	600
R_{back} (%)	61·5
FSRV (cm/s)	60 000
Grid shading (%)	~4–4·5% (for 75–85 μm gridlines)
Modeled V_{oc} (mV)	640·3
Modeled J_{sc} (mA/cm^2)	37·3
Modeled FF	0·796
Modeled η (%)	19·0

to be $\sim$170 fA/cm^2 for the textured p-type 0·6 Ωcm cell with a BSRV of 600 cm/s and a bulk lifetime of $\sim$250 μs.

Since $J_{o1} = J_{oe} + J_{ob}$, the emitter saturation current density J_{oe} was determined by subtracting the J_{ob} value from J_{o1}. This gave a J_{oe} value of $\sim$270 fA/cm^2 for the 19% efficient textured cell and 220 fA/cm^2 for 17·5% efficient planar cell.

The above analysis shows that the planar 100 Ω/sq emitter cells are still dominated by the emitter because $J_{oe} = 220$ fA/cm^2 and $J_{ob} = 162$ fA/cm^2. This is also true for the textured 100 Ω/sq cells where the emitter saturation current density is $J_{oe} = 267$ fA/cm^2 and $J_{ob} = 166$ fA/cm^2.

The total emitter saturation current density can be approximated by:[16]

$$J_{oe} = F_m J_{oem} + (1 - F_m) J_{oeSiN} \tag{5}$$

where F_m is the metal grid area coverage fraction, J_{oem} is the emitter saturation current density underneath the metal grid, and J_{oeSiN} is the emitter saturation current density of the nitride passivated emitter between the grid lines. In this study, J_{oeSiN} was measured to be 115 fA/cm^2 and $\sim$66 fA/cm^2 for textured and planar emitters respectively, using the PCD lifetime measurement[17] on a sample which was diffused and nitride coated on both sides. The metal coverage, F_m, was estimated at $\sim$0·04 for the 75–85 μm grid lines printed with PV168 paste on high sheet-resistance emitters. This gave a J_{oem} value of 3915 fA/cm^2 for the textured and 3916 fA/cm^2 for planar emitter, which is in good agreement with the J_{oem} of 4000 fA/cm^2 obtained by Lenkeit *et al.* on a 100 Ω/sq planar emitter.[16] Once J_{oeSiN} and J_{oem} are known, the total emitter recombination current density, J_{oe}, can be plotted as a function of the metal grid area fraction, F_m, for both planar and textured cells (Figure 7). Since the J_{ob} value is $\sim$170 fA/cm^2 for all the emitters, the total J_{o1} can be calculated for different J_{oe} values, from which V_{oc} can be obtained according to $V_{oc} = kT/q \cdot \ln(J_{sc}/J_{o1} + 1)$. These calculations neglect the influence of junction leakage J_{o2} on V_{oc}. This approach in Figure 7 gave a V_{oc} value of 651 mV for $F_m = 0{\cdot}04$, which is slightly higher than the experimental value of $\sim$645 mV. This difference is attributed to the influence of J_{o2} or junction leakage on V_{oc}. This approach in Figure 7

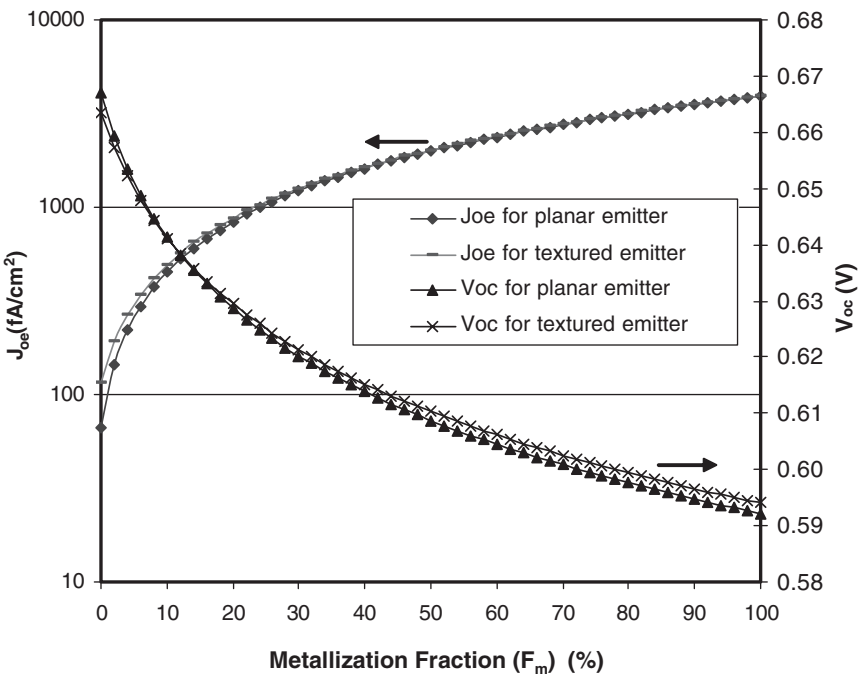

Figure 7. The effect of the metal grid percent coverage on the emitter saturation current density for planar and textured emitters

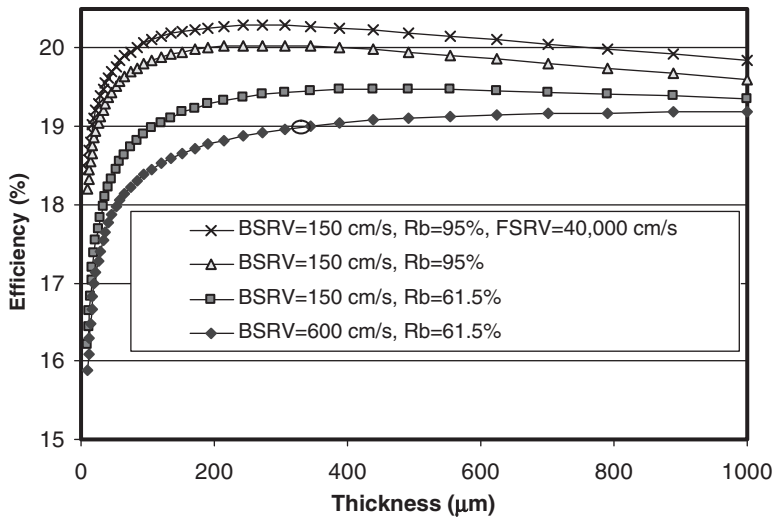

Figure 8. Efficiency versus cell thickness for different BSRV and back reflector (R_b) values for a textured cell. Results are also shown when the FSRV is reduced from 60 000 cm/s to 40 000 cm/s. The circle indicates the current status of 19% cell

shows that the maximum V_{oc} without the influence of metal ($F_m = 0$) is $\sim$663 mV for the textured and $\sim$669 mV for the planar cells with 100 Ω/sq emitter. Hence, the SP metal grid is responsible for $\sim$12 mV loss in V_{oc} for textured high sheet-resistance emitter cells.

Model calculations were extended further to project the efficiency of SP cells. Figure 8 shows the efficiency of SP cells as a function of cell thickness and process enhancement. The 19% cell is mapped on this figure. According to these calculations, the 19% cell efficiency can be raised to over 20% by a combination of improved BSRV from 600 to 150 cm/s, improved back surface reflectance (R_b) from 61.5% to 95%, and improved FSRV from 60 000 to 40 000 cm/s. These can be achieved by further improving the front and rear SP contact technology.

4. CONCLUSIONS

In conclusion, an optimized co-firing process was developed for SP contacts on textured cells which resulted in a high FF of 0·784 on 100 Ω/sq textured emitter and a high cell efficiency of 19·0%. These results were primarily made possible due to the high quality contacts resulting in a low series resistance, low junction leakage, and a high FF. The V_{oc} was also maintained at a reasonably high value of 640–644 mV for the SP textured cells on 100 Ω/sq emitter, which indicates that high quality contacts with low junction recombination and acceptable front-surface passivation were achieved. The textured surface also showed more robustness in achieving consistently low series resistance compared with the planar emitter surface. Our model calculations indicate that improving the FSRV from 60 000 cm/s to 30 000 cm/s would increase the cell efficiency to $\sim$19·3% and the use of a 95% back reflector in conjunction with a lower BSRV ($\sim$150 cm/s) can drive the SP cell efficiency above 20%. At this point, reduction in the substrate thickness from 300 to 150 μm will have no harmful effect on the cell performance, but it could lead to significant cost reduction.

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